REMARKS

Claims 12-21 are pending in this application. Favorable reconsideration of this application, in light of the following discussion, is respectfully requested.

Claims 12-14 and 16-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Kishino et al.* (U. S. Patent 6,133,678, hereinafter *"Kishino"*), in view of Applicant's prior art (figures 1-2e, hereinafter "*APA*").

Applicant respectfully traverses the above rejections under 35 U.S.C. §103(a), for the reasons discussed below, and requests reconsideration of rejected claims 12-14 and 16-21.

The outstanding Action states that it would have been obvious to a person of ordinary skill in the art to combine the fabrication method for a field emission display cathode plate having an internal via as taught by *Kishino* with the steps of sloping the plate at a predetermined angle between 10-20 degrees and forming the microtips by vertical layer evaporation as taught by *APA*. Applicant respectfully disagrees and submits that obviousness has not been shown.

For reference, current independent claim 12 of the present application is restated below:

Claim 12: "A fabrication method for the Field Emission Display (FED) cathode plate with an internal via, comprising the steps:

...

etching the gate line and the dielectric layer to form a cathode plate with a cavity of microtip, a hole upon the cavity of microtip, an internal via, and a contact;

...."

According to independent claim 12, a dielectric layer and a gate line are etched to simultaneously form an internal via and microtip cavities by one etching process. However, *Kishino* does not teach the internal via and the patterned gate line being simultaneously formed by etching the gate line and the dielectric layer through a single etching process. In contrast, the subject matter disclosed in *Kishino*, column 7 lines 13-23, teaches the internal via and the patterned gate line being formed by two different etching processes. Accordingly, Applicant respectfully submits that the outstanding Action has mischaracterized the subject matter disclosed in *Kishino*.

In particular, *Kishino* discloses a method of fabricating a field emission display cathode plate with an internal via, comprising the following steps. First, referring to Fig. 1 of *Kishino*, cathode conductors and a tape line are formed on a substrate by patterning a metal thin film, and a resistive layer is formed to cover the cathode conductors, as disclosed in column 7, lines 4-13 of *Kishino*. Next, a dielectric layer is formed on the above and then is patterned to form an internal via by a first etching process, as disclosed in column 7, lines 13-17 of *Kishino*. Finally, a gate line is formed on the dielectric layer and connected to the tape line through the internal via, and gate electrodes are formed by patterning the gate line and the dielectric layer through a second etching process, as disclosed in column 7, lines 18-23 of *Kishino*, wherein the gate electrodes are spaced by microtip cavities.

Applicant respectfully notes that in order to establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all of the claim limitations (MPEP 2143).

As noted above, neither *Kishino* nor *APA*, when taken alone or in combination, teaches forming the internal via and patterning the gate line simultaneously by etching the gate line and the dielectric layer through the same etching process, as defined in independent claim 12 of the present application.

As discussed above, the prior art references, even if combined, fail to teach or suggest all the claim limitations. Applicant submits that one having ordinary skill in the art cannot obtain the fabrication method for the field emission display cathode plate as described in claim 12 of the present application even when applying the fabrication method for the field emission display cathode plate as taught by *Kishino* to the *APA*'s method of sloping the plate at a predetermined angle between 10-20 degrees and forming the microtips by vertical layer evaporation.

Please again refer to current claim 12 as restated below:

"Claim 12. A fabrication method for the Field Emission Display (FED)cathode plate with an internal via, comprising the steps:

...

sequentially forming a dielectric layer and a gate line on the resistive layer and the tape line;

etching the gate line and the dielectric layer to form a cathode plate with a cavity of microtip, a hole upon the cavity of microtip, an internal via, and a contact;

...."

Applicant further notes that independent claim 12 recites the gate line and the dielectric layer sequentially formed on the resistive layer and the tape line before the formation of the internal via. Additionally, in the present application, the internal via is formed by etching the dielectric layer

and the tape line. To the contrary, as disclosed in *Kishino*, column 7 lines 13-23, the gate line is formed after the formation of internal via, and the internal via is formed by etching the dielectric layer. This, again, teaches away from the claimed invention because the instant claims, as defined, form the internal via and microtip cavities after the formation of the gate line.

For the reasons discussed above, Applicant respectfully submits that claim 12 is allowable over *Kishino* in view of *APA* . Insofar as claims 13-14 and 16- 21 depend from claim 12, Applicant further submits that these claims are also allowable.

Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Kishino*, in view of *APA*, and further in view of *Baldi et al*. (U. S. Patent 6,000,980, hereinafter *"Baldi"*).

Applicant respectfully submits that *Baldi* does not compensate for the above-discussed deficiencies of *Kishino* and *APA*. Therefore, Applicant submits that claim 15 is also allowable for the reasons stated above.

In addition to responding to the specific points raised by the outstanding Action, Applicant further notes that the claimed invention provides the following advantages over the cited references: (1) Only one etching process is needed to form the internal via and microtip cavities and pattern the gate line. This simplifies the processing complexity and reduces the processing cost. (2) Since one etching process of this application substitutes for two different etching processes disclosed in *Kishino*, the processing interference induced by different etching processes does not occur in this application during the process of forming the internal via and the microtip cavities and patterning the tape line.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 50-2394.

Respectfully submitted,

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